COC

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WELCOME to 2003 ICEP

On behalf of the Conference Organizing Committee, I cordially welcome you to 2003 International Conference on Electronics Packaging (ICEP) which is jointly sponsored by IEEE CPMT (Components, Packaging, and Manufacturing Technology) Society Japan and IMAPS Japan (International Microelectronics and Packaging Society Japan) / JIEP (Japan Institute of Electronics Packaging). We will provide you with a way to integrate the existing diversity of microelectronics packaging technologies. Don't miss this valuable opportunity to add the latest information to your research and development activities or professional skills.

In the Conference, invited speeches concerning the leading edge technologies both in U.S.A. and Europe will be given. Sessions for individual technologies like 3D packaging, Advanced packaging, Substrate, LTCC (low temperature co-firable ceramics), Materials, Lead-free solders, Plating, Flip-chip technologies, Design and Testing, Thermal management, Reliability, etc. with many papers will be presented for your choice.

In addition to the conference, the "Microelectronics Show" will be held at "Tokyo Ryutsu Center" which provides you with the latest information on materials, equipment and commercialized technologies in the field of your interest.

I would like to express my heartiest gratitude to the entire Organizing Committee members who have worked hard to make this Conference the most successful event. It will be a valuable opportunity you won't want to miss. See you at Tennoz Isle in Tokyo!

Kaoru Hashimoto

Kaoru Hashimoto
General Chairperson
2003 ICEP

Superfine Pitch Ultrasonic Bonding Technology on 3D Stacked LSI

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Abstract

Microbump interconnection on the through-hole electrodes is the leading technology for 3D stacked LSI. For the advanced bonding technology at low temperature, ultrasonic flip-chip bonding (UFB) was evaluated on the chip-on-chip (COC) structure. We utilized electroplated Au bumps in a 20μm-pitch to establish the optimal basic bonding conditions. The bonding temperature was kept at 150°C and the ultrasonic amplitude of the bonding tool was set at 3μm. First, the electrical test was performed and no defects were found. Then, the bonding accuracy was measured at the acceptable positional tolerance of within +/-2μm. Moreover, no bonding damage, particularly around the aluminum pads, was found. Therefore, the UFB process was realized as a low-temperature bonding process for the superfine pitch flip-chip interconnection.

Then, the measurement of the ultrasonic amplitude during the bonding process was executed with the aim of elucidating the ultrasonic bonding mechanism. This was achieved by measuring the ultrasonic amplitude of the chip and the interposer simultaneously during the bonding process, utilizing two noncontact laser vibrometers. Consequently, it became clear that the slippage between the bonding tool and the chip influenced the transmission of the ultrasonic vibration. The relative amplitude between the chip and the interposer was about 0.1μm, and it was considered that this was considerably small compared with an amplitude of 3μm of the bonding tool. However, this value was sufficient for the bonding between the chip and the interposer. Additionally, it was shown that the ultrasonic tool amplitude of 3μm did not influence the bonding accuracy, which is within +/-2μm.

1. Introduction

The national project "Ultrahigh-Density Electronic System Integration" began in 1999. This is the first project to focus on the integration of electronic devices and systems in Japan. Behind the trend, the demand for high-density electronic components is quite general for consumer information equipment. [1] New packaging technologies are required to make a break through beyond the performance limitations of the conventional package. The three-dimensional (3D) chip-stacking technologies realize the shortest wiring length between thin Si chips. Figure 1 shows a cross-section of a chip-stacked 3D LSI structure. The exposed electrodes are arranged in a 20μm-pitch on the back surface of each device. In addition, copper electrodes are formed through the 50μm-thick Si devices at a 20μm-pitch. [2]

The superfine flip-chip interconnection is also an essential technology for achieving high-speed electrical transmission. The minute electrodes on the device decrease the unproductive area in the active circuit. Moreover, the fine interconnections reduce the chip area, which leads to cost reductions and a shortened electrical path in the plane.

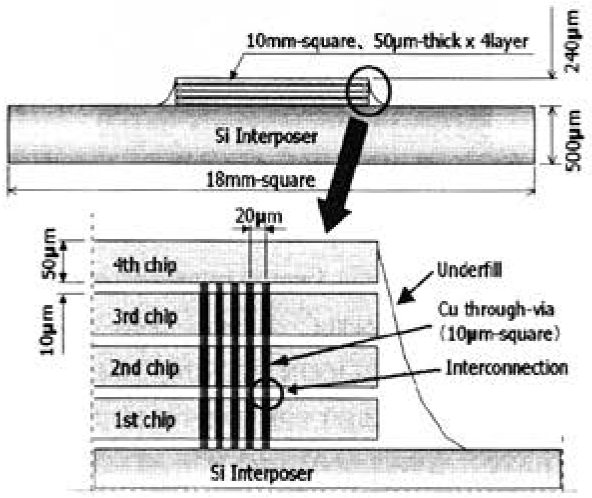

Fig. 1 A chip-stacked 3D LSI structure.

Recently, regarding the superfine flip-chip interconnection technology, it has been clarified that the UFB process is highly effective for low-temperature and low-stress interconnections. In addition, regarding the superfine pitch microbump interconnection in the UFB process, the bonding mechanism has been elucidated in metallurgical studies by observing the contact area at an atomic level. [6]-[9] However, the dynamic behavior of the UFB process phenomenon has not been examined sufficiently closely.

On the other hand, by using semiconductor strain gauges, Hizukuri et al. [10] and Watanabe et al. [11],[12] clarified the dynamic bonding behavior on the bonding area by measuring the dynamic strain on the bonding surface between the chip and the substrate in the UFB process. However, this method is not widely applicable, because it is necessary to use a special substrate and chip.

In this paper, first, the results of the experiments are introduced, which focus on the feasibility of the UFB process for utilizing electroplated Au bumps in a 20μm-pitch. Next, we present the measurement of the ultrasonic amplitude during the UFB process which was executed with the aim of elucidating the ultrasonic bonding mechanism.

As a result, it is clarified that the slippage between the bonding tool and the chip influenced the transmission of the ultrasonic vibration. This was achieved by measuring the ultrasonic amplitude of the chip and the interposer simultaneously during the bonding process, utilizing two noncontact laser vibrometers.

2. Evaluation of Bondability
2.1 COC structure and bonding conditions

For the advanced microbump interconnection, the UFB process was evaluated on electroplated Au bumps in a 20μm-pitch formed on the aluminum pads. Figure 2 shows the COC structure constructed with the Si chip and the Si interposer. The Si chip size was 10mm-square and 50μm-thick. The bump size was 12μm-square and 7.5μm in height, and 1844 bumps were located on the periphery of the Si chip. The Si interposer size was 18mm-square and 500μm thick. The bumps on the interposer were located in the opposed adjustment as the Si chip in a 20μm-pitch.

Figure 3 shows the experimental model for the bondability evaluation of the UFB process. First, the bump surface of both the chip and the interposer was cleaned by argon sputtering. The etching condition was set at 30 nm in depth. The chip and the interposer were fixed to the bonding tool and the bonding stage respectively by air vacuum. We adopted the bonding tool of which the surface had been coated to 0.5μm thickness by fluoroplastics. Regarding the bonding conditions, the bonding temperature was kept at 150°C and the ultrasonic amplitude of the bonding tool was set at 3μm, and the bonding forces were set at 20N.

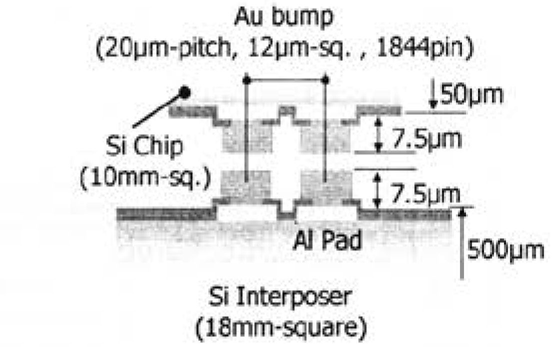

Fig. 2 COC structure for evaluation of UFB.

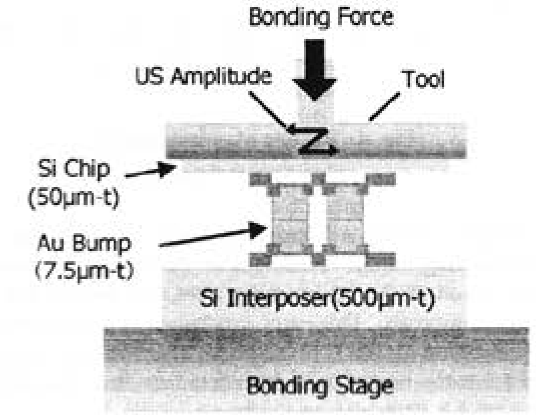

Fig. 3 Experimental model for bondability evaluation of UFB.

2.2 Evaluation results for bondability

Figure 4 shows the results of the electrical test after the bonding with the optimal basic bonding conditions. For defect detection, we used the daisy chain pattern method. As a result, the resistance of the interconnection was stable and no defects were found.

Figure 5 shows the results of the measurement on the positional tolerance. Mark 1 was formed at the upper right corner and Mark 2 was formed at the diagonal corner on the Si chip for alignment. As a result, the bonding accuracy was confirmed within +/-2μm. This confirms that a 20μm-pitch UFB process is suitable for application in manufacturing. There was some concern that the ultrasonic oscillation would have some influence on positional accuracy. However, the measured bonding accuracy was comparable to the positional tolerance of the UFB bonding machine. Therefore, the actual oscillation of the chip was assumed to be considerably smaller than the tool amplitude.

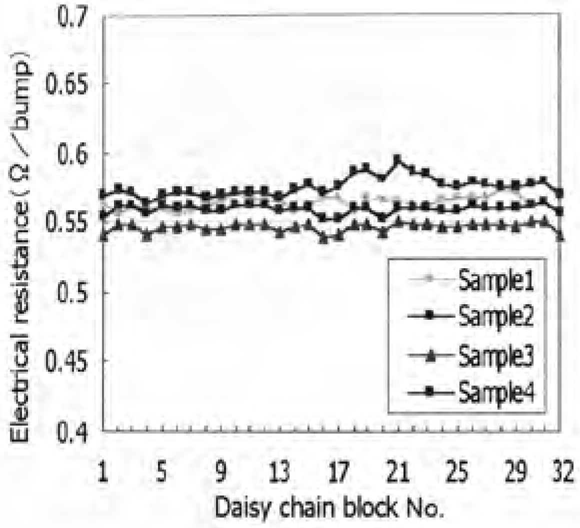

Fig. 4 Results of measurement of electrical resistance.

Figure 6 shows a micrograph of the cross-section of a Au bonding bump. As shown in the figure, no damage was found at the interface between the bumps and the aluminum pads. This was confirmed by under-bump-metalization (UBM). In addition, the bonding interface between the bumps was considered as fine, because no remarkable defects were observed.

As described above, the fundamental bondability of the UFB process was confirmed with a 20μm-pitch. It was also necessary to verify the detailed mechanism of the ultrasonic transmission and the friction of the interface, for evaluating the bondability.

3. Evaluation of ultrasonic oscillation

3.1 Measurement method of ultrasonic oscillation

In this research, the measurement of the ultrasonic amplitude during the UFB process was executed with the aim of elucidating the ultrasonic bonding mechanism.

Figure 7 shows the method for the measurement of the ultrasonic amplitude in the UFB process. The ultrasonic vibration measurement system is shown in figure 8. As shown in this figure, in order to determine the relative amplitude between the chip and the interposer, we used two noncontact laser vibrometers ("OFV-2600/502-1", "OFV-3000/502", Polytec Inc.) to measure the ultrasonic oscillation of both the right and left sides of the specimen simultaneously during the UFB process. In addition we performed a computer analysis of the oscillation wave.

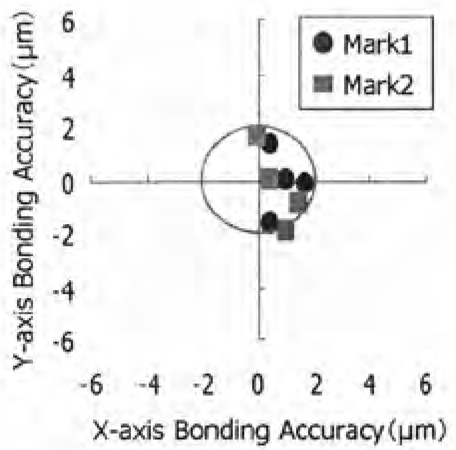

Fig. 5 Results of measurement of positional tolerance.

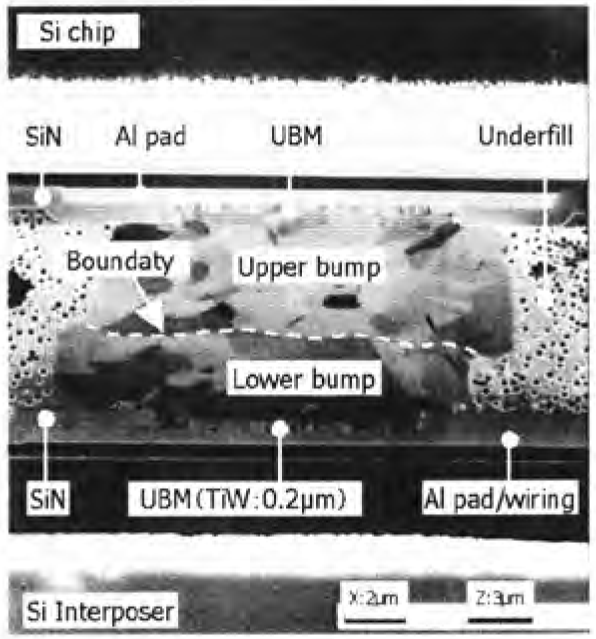

Fig.6 Micrograph of microjoint.

We used the ultrasonic flip-chip bonding machine ("SH50M", ULTEX Co.) to evaluate the ultrasonic oscillation. To measure the ultrasonic vibration of the chip utilizing the laser vibrometer, we used the chip of a specification different from that used for the bondability evaluation described in the previous section.

For the purpose of easily setting the focus of the laser to the side of the Si chip, we used a 500μm-thick Si chip instead of a 50μm-thick Si chip. Moreover, to position

the Si chip onto the Si interposer manually, we used a 0.5μm-thick Au plated Si chip instead of a Si chip with 7.5μm-high Au bumps.

The ultrasonic oscillation wave measured with the laser vibrometer was recorded with the digital oscilloscope ("TDS744A", Tektronix Inc.). Because the ultrasonic frequency was 50kHz, we adopted 2μs as the sampling period. Therefore, for the measurement of both the chip and the interposer, the volume of data of the acquisition wave in each measurement reached 500,000 points.

The acquisition wave was also analyzed with the numeric processing software ("CUT Ver.8.1", Evergreen Co.). Then, the oscillation wave velocity was converted into the amplitude. Finally, the relative amplitude of the chip and the interposer was detected with high accuracy.

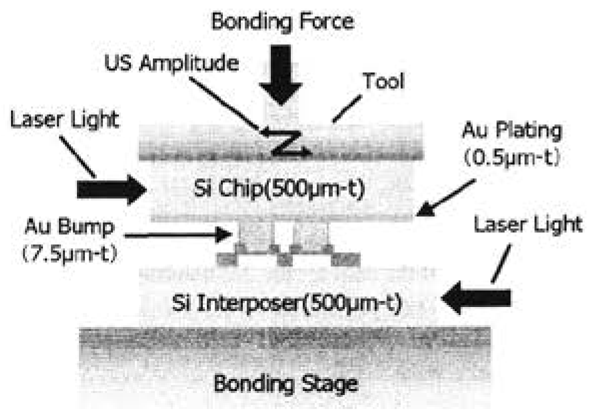

Fig. 7 Measurement of the ultrasonic amplitude of UFB.

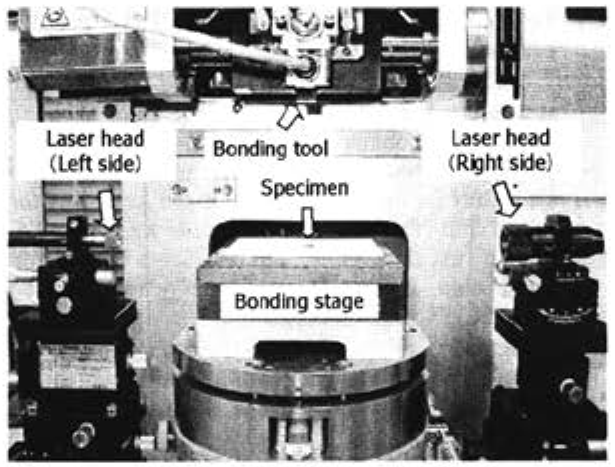

Fig. 8 Ultrasonic vibration measurement system

3.2 Evaluation results for ultrasonic amplitude

In this evaluation, the bonding temperature was kept at 150°C and the ultrasonic amplitude of the bonding tool was set at 3μm. The bonding force and bonding time were set at 30N and 300ms, respectively. The argon sputtering time, the bonding tool materials, the fixing method of the chip and the interposer and other conditions were the same as those of the bondability evaluation described in the previous section. Figure 9 shows the original oscillation wave of both the chip and the interposer during the bonding. Figure 10 shows the time-domain-zooming waves of the original waves of both the chip and the interposer. As shown this figure, the shape of the oscillation waves of both the chip and the interposer was a sine wave of 50 kHz, and the phase of both waves was almost the same.

Figure 11 shows the peak-to-peak amplitudes of both the chip and the interposer, which were analyzed with the numeric processing software. As the figure shows, the peak-to-peak amplitude of the chip was about 0.5μm. This value was very small compared with the setting amplitude of the tool of 3μm. On the other hand, the analyzed peak-to-peak amplitude of the interposer was slightly smaller than that of the chip.

The relative amplitude between the chip and the interposer is shown in figure 12. Because of slippage between the tool and the chip, and slippage between the chip and the interposer, the relative amplitude of 0.1μm between the chip and the interposer was very small compared with the amplitude of 3μm of the tool.

However, this relative amplitude was sufficient for satisfactory bonding between the chip and the interposer. Additionally, it was shown that the ultrasonic tool amplitude of 3μm did not influence the bonding accuracy, which is within +/-2μm.

To increase our understanding of the ultrasonic bonding mechanism, we executed the same bonding process using the sample which completed the bonding. Figure 12 shows the relative amplitude between the chip and the interposer in this case. We assumed that the relative amplitude of 0.03 - 0.07μm was caused by the elastic or plastic deformation of the bump.

To verify the accuracy and effectiveness of our adopted measurement method of the ultrasonic oscillation, the vibration of the right and left sides of the same chip was measured simultaneously during the UFB process.

Figure 13 shows the relative amplitude between the right and left sides of the chip during the UFB process. As shown in the figure, because the amplitudes of the two sides almost corresponded, we verified that this measurement method has high accuracy.

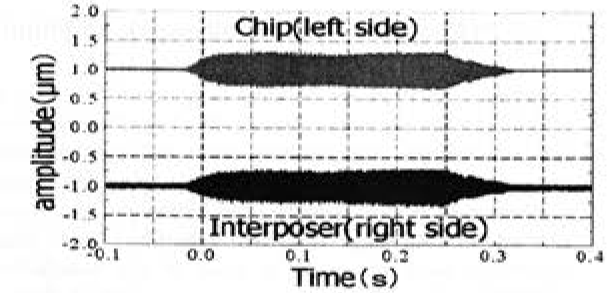

Fig. 9 Measured original oscillation wave.

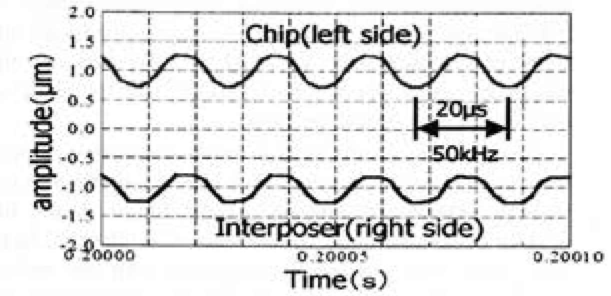

Fig. 10 Time-domain-zooming wave.

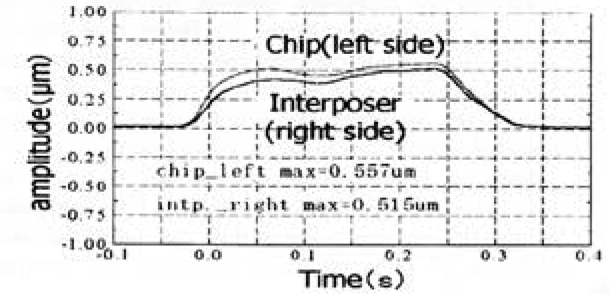

Fig. 11 Peak-to-peak amplitude using a wave processor.

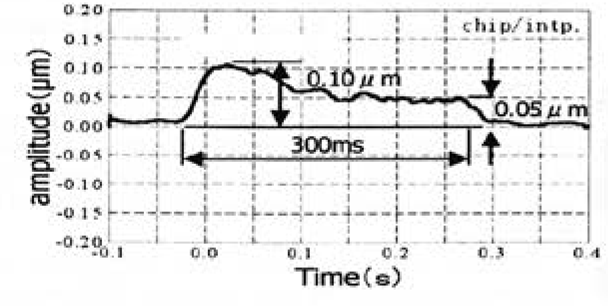

Fig. 12 Relative amplitude between chip and interposer for the initial bonding process.

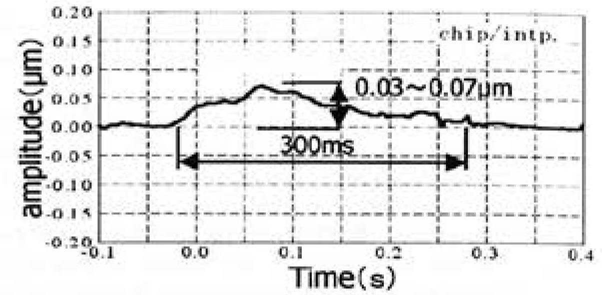

Fig. 13 Relative amplitude between chip and interposer for the 2nd bonding process.

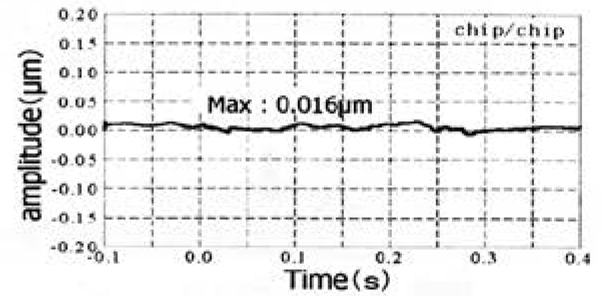

Fig. 14 Relative amplitude between right and left sides of the chip for the 3rd bonding process.

3.3 Initial evaluation of multistacked COC structure with UFB

In the previous section, we demonstrated the effectiveness of the UFB process on a COC structure with a superfine pitch microjoint.

Then, we began the examination of the UFB technology for the multistacked LSI. The initial evaluation results are presented below.

The cross-sectional SEM image of a 4-chip stacked structure is shown in Figure 15. The chips have 20μm-pitch Au microbumps and the chip is 50μm-thick. The chips were sequentially bonded. The bonding force was set at 20N for the first three chips, and set at 30N for the fourth chip. The ultrasonic amplitude was set at 1.5 μm for the first three chips, and was set at 3.0μm for the fourth chip. In addition, the bonding temperature was kept at 150°C for every layer.

Figure 16 shows a magnified photograph of the stacked LSI. As shown in these figures, we confirmed that the positional accuracy of bonding and the bump deformation characteristic were suitable.

We plan to optimize the multistacked LSI bonding process in the near future.

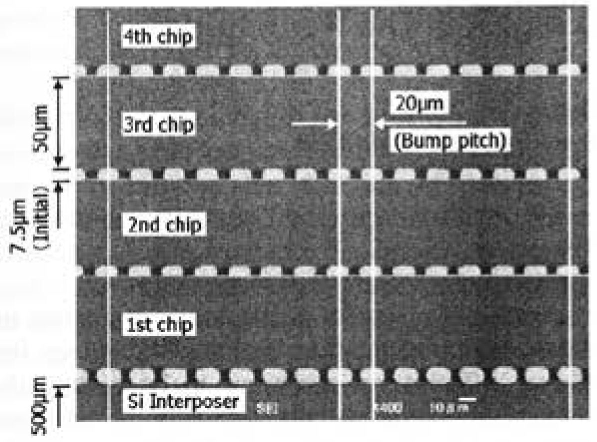

Fig. 15 3D stacked LST using UFB.

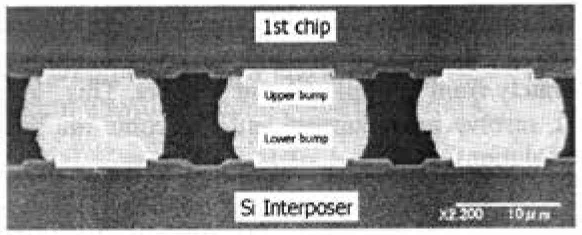

Fig. 16 Microjoint of 3D stacked LSI using UFB.

4. Conclusion

In this research, the following conclusions were obtained with respect to the utilization of superfine pitch UFB technology on the COC structure.

(1) For the COC structure to have a microbump of 12μm-square and 7.5μm-height, it was shown that a comparatively large amplitude of the tool of 3μm was necessary for satisfactory ultrasonic bonding.

(2) To determine the relative amplitude between the chip and the interposer, we used two noncontact laser vibrometers to measure the ultrasonic oscillation of both the right and left sides of the specimen simultaneously during the UFB process. In addition we performed a computer analysis of the oscillation wave.

(3) Because of slippage between the tool and the chip, and slippage between the chip and the interposer, the relative amplitude of about 0.1μm between the tool and the chip on the bonding area is very small compared with the amplitude of about 3μm of the tool.

(4) Therefore, the UFB process is potentially an effective bonding method for bonding COC structures at or below a 20μm-pitch.

Acknowledgments

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